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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,315	02/09/2004	Naoki Kuroda	60188-762	6654

7590 08/11/2006

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,315	KURODA ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,6-35,37 and 38* is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *28 June 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment received on 6/28/2006 has been reviewed and considered with the following results:

As to the prior art rejection to the claims, made in the previous Office Action mailed on 02/28/2006, Applicant's arguments have been carefully reviewed, but are not persuasive. The arguments supporting the previous rejections are addressed in detail below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 4, 5, and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Mizuno (US 6,396,323; previously cited).

With regard to claim 1, Mizuno discloses in Figs. 3-9 a semiconductor device comprising first circuit block and second circuit block (110a & 110b) provided on a single semiconductor chip (100) and including respective functional elements; and a timing adjustment circuit block (111a & 111b) provided on the single semiconductor chip between the first and second circuit

blocks for adjusting a propagation timing of a transmission signal flowing on a line connecting the first and second circuit blocks to each other.

With regard to claim 2, the semiconductor device further comprises a comparison control circuit (401) for receiving an input signal input to the first circuit block and an output signal output from the second circuit block which has received the transmission signal, comparing the input signal to the output signal, and controlling the timing adjustment circuit block.

With regard to claim 4, the reference also meets the recited limitations in the claim.

With regard to claim 5, the semiconductor device further comprises an input pattern generating circuit (101) for generating and outputting the input signal to the first circuit block. With regard to claim 36, the second circuit block is a memory circuit block (by given the broadest reasonable interpretation; the circuit block 408 is a memory circuit block because it has a function of storing a signal).

Response to Arguments

4. Applicant's argument stating that "Mizuno does not disclose or suggest a timing adjustment circuit block for adjusting a propagation timing of a transmission signal flowing on a line connecting the first and second circuit blocks to each other, but rather than adjusting the phases of clocks, each of which being respectively provided for the macros 110a and 110b from a clock buffer 103". That argument is not persuasive because Fig. 9 of Mizuno clearly showing a line connecting the first and second circuit blocks to each other, i.e. from 110a through 111a, 103, 111b, and then to 110b. By given the broadest reasonable interpretation, that line connects the first and second circuit blocks to each other. Furthermore, "adjusting the phases of clocks"

also clearly meets the claimed limitation "adjusting a propagation timing of a transmission signal". For example, the clock (clock signal) should be understood within the art as the transmission signal, and "adjusting the phases of clocks" should be understood within the art as "adjusting propagation timing of the clock signals". Indeed, Arcus discloses in Figs. 2-7 (see US Patent No. 6,426,662) that adjusting the phases of clocks by adjusting propagation timing of the clock signals. Accordingly, Mizuno clearly anticipates all the recited limitations of the claim, and therefore the rejections of record are still believed to be proper.

Allowable Subject Matter

5. Claims 3, 6-35, 37 and 38 are allowed.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 1), as recited in claim 3, having specific structural limitation such as the line (DAs) comprises a plurality of parallel lines (DA1, DA2 in instant Fig. 3), and each of the first and second circuit blocks (11 and 12 in instant Fig. 1),) includes a shift register (14, 15) connected to the plurality of lines, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 1), as recited in claim 11, having specific structural limitation such as the comparison control circuit (19) includes a control circuit (18) for outputting timing adjustment control signals (CNT) to the timing adjustment circuit block (13) when the comparison result shows that the input signal (16) and the output signal (OUT) differ from each other, the timing adjustment circuit block (13 in instant Fig. 3) includes a counter circuit (32) for receiving the timing

adjustment control signals (CNT), and counting and electrically holding the number of the received timing adjustment control signals; a delay element block (31) which includes at least one delay element and in which a delay amount depending on the number of the timing adjustment control signals is added to the transmission signal; and a fuse circuit (33) which includes at least one fuse and holds the number of the timing adjustment control signals in correspondence with the number of fuses which are melted down, wherein an output signal from the counter circuit or an output signal from the fuse circuit is selectively input to the delay element block, and the fuse is melted down based on the output signal from the counter circuit, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 1), as recited in claim 6, having specific structural limitation such as the timing adjustment circuit block (13 in instant Fig. 3) includes a first holding circuit (32, 33) for holding update information (CNT) in which the propagation timing of the transmission signal is updated, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 1), as recited in claim 21, having specific structural limitation such as the timing adjustment circuit block (50 in instant Fig. 11) includes a determination period signal generating circuit (51's) for generating and outputting a determination period signal (CSH's) for determining the propagation timing of the transmission signal, based on a clock signal (CLK) for determining the propagation timing of the transmission signal; a delay element block (31's)

which includes at least one delay element and in which a delay is added to the transmission signal (DA1, DA2); and a fuse circuit (33's) which includes at least one fuse, the fuse being melted down based on the determination period signal and a transmission signal which has passed through the delay element block, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 13), as recited in claim 27, having specific structural limitation such as the input pattern generating circuit (61, 62) for generating and outputting the input signal (IN2) to the first circuit block (11), wherein the input pattern generating circuit is activated when the comparison result (1) from the comparison control circuit (19) shows that the input signal and the output signal (OUT2) differ from each other, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 14), as recited in claim 32, having specific structural limitation such as the comparison control circuit (19) includes a control circuit (18) for outputting timing adjustment control signals (CNT) to the timing adjustment circuit block (13) when the comparison result shows that the input signal (IN2) and the output signal (OUT2) differ from each other, the timing adjustment circuit block (70 in instant Fig. 15) includes a counter circuit (32) for receiving the timing adjustment control signals, and counting and electrically holding the number of the received timing adjustment control signals; a delay element block (31) which includes at least one delay element and in which a delay amount depending on the number of the timing adjustment control signals is added to the transmission signal; and a nonvolatile memory circuit

(71), wherein. an output signal from the counter circuit or an output signal from the nonvolatile memory circuit is selectively input to the delay element block, and the number of the timing adjustment control signals is written into the nonvolatile memory circuit based on the output signal from the counter circuit, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 7), as recited in claim 37, having specific structural limitation such as the output timing changing circuit (43, 44 in instant Fig. 8) for changing the timing of outputting (DOUTD) an output signal (DOUT) from the memory circuit block in synchronization with a change of the propagation timing (42) of a clock signal (CLK to CLKD) for determining the propagation timing of the transmission signal (DAs), and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
August 3, 2006

QUAN TRA
PRIMARY EXAMINER